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APPENDIX SHOWING CHANGES MADE TO SPEC AND CLAIMS

In the Specification

[0037] Referring again to FIG. 9, the connection bars 78 and 79 intersect at a point between the four die 70-76. The first (inner) rows of terminals are attached to the connection bars 78, 79 through grooved connection interfaces 77 in a manner such as that shown in the drawing. The leadframe panel 60 is preferably formed from a sheet of conductive metal having a good thermal conductivity, such as copper. The leadframe panel 60 may be formed by a stamping method, however, for more complex and higher density leadframes, a chemical etching method is preferred. As is understood by those of skill in the art, the etching method uses an artwork mask to define the detailed pattern of the leadframe and then the unmasked portion of the metal is etched away. A plating mask is used to mask out no-plating zones, if any, and then the unmasked portions are plated with metal layers with a plating process. Rinsing and cleaning steps are performed between processes. Such masking, etching, plating, rinsing and cleaning processes are well known to those of skill in the art.

In the Claims

1. (Twice Amended) A leadframe for a semiconductor device, the leadframe comprising:

a paddle ring having an inner perimeter, an outer perimeter, and a cavity located within the inner perimeter for receiving an integrated circuit die~~,~~ , the paddle ring outer perimeter including outwardly extending leads that terminate in a first row of terminals generally surrounding the paddle ring outer perimeter~~, wherein each of the terminals of the first row of terminals is individually connected to the paddle ring~~; and

a second row of terminals surrounding the first row of terminals, wherein each of the terminals of the second row of terminals is connected to a connection bar and wherein the ~~inner~~ first row of terminals is connected to the ~~outer~~ second row of terminals at a corner of the connection bar.

9. (Twice Amended) The leadframe of claim 8, further comprising another row of terminals connected to ~~the other~~ a first side of the connection bar opposing a second side of the connection bar to which the second row of terminals is connected, said another row of terminals for connecting to a second integrated circuit die.

12. (Twice Amended) A semiconductor device, comprising:

a paddle ring having an inner perimeter, an outer perimeter, and a cavity located within the inner perimeter~~,~~ , the paddle ring outer perimeter including outwardly extending leads that terminate in a first row of terminals generally surrounding the paddle ring outer perimeter ~~,~~ ~~wherein each of the terminals of the first row of terminals is individually connected to the paddle ring and extends outwardly therefrom~~;

a second row of terminals surrounding the first row of terminals, wherein each of the terminals of the second row of terminals is connected to a connection bar and wherein the ~~inner~~ first row of terminals is connected to the ~~outer~~ second row of terminals at a corner of the connection bar; and

an integrated circuit die placed within the cavity and surrounded by the paddle ring, the die including a plurality of die pads that are electrically connected to respective ones of the terminals of the first and second rows of terminals.

END OF APPENDIX